# Detailed Curriculum for Master of Technology (M. Tech.) in VLSI and Embedded Systems

## Semester - I

| Course Code | Course Type | Course Name | L | T | P | Credit | Total Marks |
|---|---|---|---|---|---|---|---|
| MVE-101C | Core-1 | RTL Simulation and Synthesis with PLDs | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-102C | Core-2 | Analog and Digital CMOS VLSI Design | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-101E | Professional Elective-1 (any one) | Digital Signal and Image Processing | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-102E | | Programming Languages for Embedded Software. | | | | | |
| MVE-103E | | VLSI signal processing | | | | | |
| MVE-104E | Professional Elective-2 (any one) | Parallel Processing | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-105E | | System Design with Embedded Linux | | | | | |
| MVE-106E | | CAD of Digital System | | | | | |
| MVE-101L | Lab-1 | RTL Simulation and Synthesis with PLDs Lab | 0 | 0 | 4 | 2 | 100 |
| MVE-102L | Lab-2 | Analog and Digital CMOS VLSI Design Lab | 0 | 0 | 4 | 2 | 100 |
| MID-101F | Computer Skills 3 (Compulsory foundation) | Python Programming | 4 | 0 | 0 | 4 | 100 *(70+30) |
| | | **Total** | **20** | | **8** | **24** | **700** |

*70(Theory) + 30(Internal Assessment)

## Semester - II

| Course Code | Course No. | Course Name | L | T | P | Credit | Total Marks |
|---|---|---|---|---|---|---|---|
| MVE-201C | Core-3 | Microcontrollers and Programmable Digital Signal Processors | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-202C | Core-4 | VLSI Design Verification and Testing | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-201E | Professional Elective-3 (any one) | Memory Technologies | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-202E | | SoC Design | | | | | |
| MVE-203E | | Low power VLSI Design | | | | | |
| MVE-204E | Professional Elective-4 (any one) | Communication Buses and Interfaces | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MVE-205E | | Network Security and Cryptography | | | | | |
| MVE-206E | | Physical Design Automation | | | | | |
| MVE-201S | Sessional-1 | Term Paper Leading to Thesis | 0 | 0 | 4 | 2 | 100 |
| MVE-202S | Sessional-2 | Design Project | 0 | 0 | 4 | 2 | 100 |
| | **Total** | | **16** | **0** | **8** | **20** | **600** |

*70(Theory) + 30(Internal Assessment)

## Semester – III

| Course Code | Course No. | Course Name | L | T | P | Credit | Total Marks |
|---|---|---|---|---|---|---|---|
| MVE-301S | Sessional-3 | Thesis Report Interim | 0 | 0 | 8 | 4 | 100 |
| MVE-302S | Sessional-4 | Thesis Seminar Interim (Presentation and Viva Voce) | 0 | 0 | 8 | 4 | 200 |
| MVE-303S | Sessional-5 | Technical Communication | 0 | 0 | 4 | 2 | 100 |
| MVE-304S | Sessional-6 | Workshop and Seminars - I | 0 | 0 | 2 | 0 | 100 |
| MVE-301E<br>MVE-302E<br>MVE-303E<br>MVE-304E | Professional Elective-5 (any one) | Interdisciplinary Open Elective Offered by Other Departments | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MID-301A | Audit Course | Research Methodology and IPR | 2 | 0 | 0 | 0 | 100 *(70+30) |
| | **Total** | | **6** | **0** | **22** | **14** | **700** |

*70(Theory) + 30(Internal Assessment)

## Semester - IV

| Course Code | Course No. | Course Name | L | T | P | Credit | Total Marks |
|---|---|---|---|---|---|---|---|
| MVE-401S | Sessional-7 | Thesis Report Final | 0 | 0 | 08 | 4 | 200 |
| MVE-402S | Sessional-8 | Thesis Seminar Final (Presentation and Viva Voce) | 0 | 0 | 08 | 4 | 200 |
| MVE-403S | Sessional-9 | Workshop and Seminars - II | 0 | 0 | 02 | 2 | 100 |
| MDS-401O<br>MDS-402O<br>MTE-401O<br>MTE-402O | Open Elective Paper (Offered by other department) | Interdisciplinary Open Elective Offered by Other Departments | 4 | 0 | 0 | 4 | 100 *(70+30) |
| MID-401F | Foundation Course | English for Research Paper Writing | 2 | 0 | 0 | 0 | 100 *(70+30) |
| MID-402F | | Disaster Management | | | | | |
| MID-403F | | Sanskrit for Technical Knowledge | | | | | |
| MID-404F | | Value Education | | | | | |
| MID-405F | | Constitution of India | | | | | |
| MID-406F | | Pedagogy Studies | | | | | |
| MID-407F | | Stress Management by Yoga | | | | | |
| MID-408F | | Personality Development through Life Enlightenment Skills | | | | | |
| | **Total** | | **6** | | **18** | **14** | **700** |

*70(Theory) + 30(Internal Assessment)

# Semester - I

# Semester – I

## Core-1

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **RTL Simulation and Synthesis with PLDs** | **MVE-101C** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Design of Finite State Machines and RTL using reconfigurable logic. |
| **CO-2** | Use EDA tools like Cadence, Mentor Graphics and Xilinx. |
| **CO-3** | Low power VLSI design techniques, their testability and performance. |
| **CO-4** | Design and develop IP cores and Prototypes with performance guarantees. |
| **CO-5** | Analyse case studies related to RTL Simulation and Synthesis with PLDs |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs. Design entry by Verilog/VHDL/FSM, Verilog AMS. |
| **MODULE-2** | Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification,<br>Power analysis, ESD protection. Design for performance, Low power VLSI design techniques. Design for testability. |
| **MODULE-3** | IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping. |
| **MODULE-4** | Case studies and Speed issues. |

**References:**


- Richard S. Sandige, "Modern Digital Design", MGH, International Editions.
- Donald D Givone, "Digital principles and Design", TMH
- Charles Roth, Jr. and Lizy K John, "Digital System Design using VHDL", Cengage Learning
- Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall.
- Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx
- Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books.


## Core-2

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| Analog and Digital CMOS VLSI Design | **MVE-102C** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Analyse, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics. |
| **CO-2** | Design and implement the logical building blocks of a VLSI system. |
| **CO-3** | Compare single and multi-stage CMOS amplifiers. |
| **CO-4** | Understanding of CMOS OP-AMP and its gain, Slew rate and PSRR. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | ***Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process*** Digital CMOS Design: Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption. Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.. |
| **MODULE-2** | Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc. |
| **MODULE-3** | Analog CMOS Design: Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell. |
| **MODULE-4** | Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques. |

**References:**


- J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
- Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
- BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
- Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd• Edition.
- R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
- Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",TMH, 3rdEdition.
- Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.


**Professional Elective-1**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Digital Signal and Image Processing** | **MVE-101E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Analyse discrete-time signals and systems in various domains. |
| **CO-2** | Design and implement filters using fixed point arithmetic targeted for embedded platforms. |
| **CO-3** | Compare algorithmic and computational complexities in processing and coding digital images. |
| **CO-4** | Develop VLSI architectures for implementation of Image Processing algorithms. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's. |
| **MODULE-2** | Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation. Fixed point implementation of filters – challenges and techniques. |

| | |
|---|---|
| **MODULE-3** | Digital Image Acquisition, Enhancement, Restoration. Digital Image Coding and Compression – JPEG and JPEG 2000. Color Image processing – Handling multiple planes, computational challenges. |
| **MODULE-4** | VLSI architectures for implementation of Image Processing algorithms, Pipelining. |

**References:**


- J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
- Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition
- S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition,2006
- A.K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
- Keshab Parhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India.


## Professional Elective-1

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Programming Languages for Embedded Software** | **MVE-102E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Write embedded C programs for interfacing peripheral devices. |
| **CO-2** | Analyse the characteristic features of object oriented programming languages. |
| **CO-3** | Develop and analyse object oriented algorithms in C++. |
| **CO-4** | Develop exceptions handing algorithms using try-catch methods. |
| **CO-5** | Develop applications using scripting languages. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Embedded 'C' Programming - Bitwise operations, Dynamic memory allocation, OS services - Linked stack and queue, Sparse matrices, Binary tree - Interrupt handling in C, Code optimization issues - Writing LCD drives, LED drivers, Drivers for serial port communication - Embedded Software Development Cycle and Methods (Waterfall, Agile). |
| **MODULE-2** | Object Oriented Programming - Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism. |
| **MODULE-3** | CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation. Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions, |
| **MODULE-4** | Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.<br>Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing. |

**References:**


- Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008

- Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011
- A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
- Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
- Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005


**Professional Elective-1**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **VLSI signal processing** | **MVE-103E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Understand about DSP algorithms, its DFG representation, pipelining and parallel processing approaches. |
| **CO-2** | Demonstrate retiming techniques, folding and register minimization path problems. |
| **CO-3** | Explain about systolic architecture design, finite word-length effects and round off noise computation in DSP systems. |
| **CO-4** | Illustrate algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Introduction to DSP systems, Pipelined and parallel processing. |
| **MODULE-2** | Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms. |
| **MODULE-3** | Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise. Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. |
| **MODULE-4** | Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design. Programmable digit signal processors. |

**References:**


- Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley,
  Inter Science, 1999.
- Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
- S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.


**Professional Elective-2**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Parallel Processing** | **MVE-104E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Explain parallel processing and pipelining. |
| **CO-2** | Analyse the performance parameters of different processor architectures. |

| | |
|---|---|
| **CO-3** | Investigate issues related to parallel programming techniques. |
| **CO-4** | Understand operating systems for multiprocessors systems. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Overview of Parallel Processing and Pipelining, Performance analysis, Scalability. Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining. |
| **MODULE-2** | VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture. Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions. |
| **MODULE-3** | Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. |
| **MODULE-4** | Operating systems for multiprocessors systems Customizing applications on parallel processing platforms. |

**References:**


- Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
- Kai Hwang, "Advanced Computer Architecture", TMH
- V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.
- William Stallings, "Computer Organization and Architecture, Designing for performance" PH, Sixth edition
- Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing", MGH
- David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann.


## Professional Elective-2

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **System Design with Embedded Linux** | **MVE-105E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Understand the embedded Linux development model. |
| **CO-2** | Develop profile applications and drivers in embedded Linux. |
| **CO-3** | Develop programs in real time Linux environment. |
| **CO-4** | Build and Debug Kernel, Root file system Embedded Graphics. |
| **CO-5** | Analyse case studies related to uClinux. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Embedded Linux Vs Desktop Linux, Embedded Linux Distributions. Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence. |
| **MODULE-2** | Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules. |
| **MODULE-3** | Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux. |
| **MODULE-4** | Building and Debugging: Kernel, Root file system Embedded Graphics. Case study of uClinux Model. |

**References:**


- Karim Yaghmour, "Building Embededd Linux Systems", O'Reilly & Associates
- P Raghvan, Amol Lad, SriramNeelakandan, "Embedded Linux System Design and Development", Auerbach Publications

- Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition, 2010.
- Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014.


**Professional Elective-2**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **CAD of Digital System** | **MVE-106E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Understand fundamentals of CAD tools for modelling, design, fabrication, test and verification of VLSI systems. |
| **CO-2** | Analyse various phases of CAD, including simulation, physical design, test and verification. |
| **CO-3** | Evaluate combinational optimization, partitioning, floor planning and high level synthesis. |
| **CO-4** | Design and implement circuits using MCMS-VHDL-Verilog. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design. |
| **MODULE-2** | VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems. |
| **MODULE-3** | General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement, routing. Simulation – logic synthesis, verification, high level Synthesis. |
| **MODULE-4** | MCMS-VHDL-Verilog-implementation of simple circuits using VHDL |

**References:**


- N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".
- S.H. Gerez, "Algorithms for VLSI Design Automation.


**Lab-1**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **RTL Simulation and Synthesis with PLDs Lab** | **MVE-101L** | **4 hrs/week** | **2** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| CO-1 | Implement combinational and sequential circuits using Verilog |
| CO-2 | Design and implementation of FSMs in Verilog |
| CO-3 | Realize functionality of SRAM in Verilog. |
| CO-4 | Demonstrate PCI Bus / UART/ USART / FFT / IFFT /implementation. |

**List of Experiments: Minimum Six experiments to be carried out.**

1) Verilog implementation of 8:1 Mux/ Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2) Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3) Vending machines - Traffic Light controller, ATM, elevator control.
4) PCI Bus & arbiter and downloading on FPGA.
5) UART/ USART implementation in Verilog.
6) Realization of single port SRAM in Verilog.
7) Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8) Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

**Lab-2**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Analog and Digital CMOS VLSI Design Lab** | **MVE-102L** | **4 hrs/week** | **2** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Design and analyze CMOS inverter using EDA tools. |
| **CO-2** | Understand the interpretation of circuit simulation results. |
| **CO-3** | Understand the impact of parameter changes through simulation. |
| **CO-4** | Design and interpret analog CMOS circuits using EDA tools . |

**List of Experiments:-**

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS =30mV
To extract Vth use the following procedure.
i. Plot gm vs VGS using ngspice or equivalent eda tools and obtain peak gm point.
ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice or equivalent EDA tools .
iii. Use Ngspice or equivalent EDA tools to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.
Tabulate your result according to technologies and comment on it.

2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
a) Perform the following
i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
ii. Plot VTC for CMOS inverter with varying VDD.
iii. Plot VTC for CMOS inverter with varying device ratio.
b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)
c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k).

3) Use Ngspice or equivalent EDA tools to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4) Perform the following
a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice or equivalent EDA tools and compare the values for 0.18um and 0.13um process.
b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.
i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.
ii. Calculate input bias voltage if bias current=50uA. iii. Use Ngspice or equivalent EDA tools and obtain the bias current. Compare its value with 50uA.
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice or equivalent EDA tools (consider 30fF load capacitance).
v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
vi. Use Ngspice or equivalent EDA tools to determine input voltage range of the amplifier.

5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note:
Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
i. Draw the schematic of op-amp macro model.
ii. Draw the schematic of INA.
iii. Obtain parameters of the op-amp macro model such that
a. low-frequency voltage gain = 5x104,
b. unity gain BW (fu) = 500KHz,
c. input capacitance=0.2pF,
d. output resistance =_,
e. CMRR=120dB
iv. Draw schematic diagram of CMRR simulation setup.
v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches. vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.

6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind or equivalent.
a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo or equivalent.
d) Use interconnect length obtained and connect the second and third inverter.
Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part ‘c’.

**Compulsory Foundation (Interdisciplinary Mandatory)**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Computer Skills 3 (Python Programming)** | **MID-101F** | **4 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | To realize basic programming skills in Python. |
| CO-2 | Explore control structures and lists in Python |
| CO-3 | To develop the ability to write functions in Python |

| | |
|---|---|
| CO-4 | To acquire programming skills for file handling in Python. |

| | |
|---|---|
| **Module-1** | Fundamental concepts: Literals, variables and identifiers, operators, expressions and data types. |
| **Module-2** | Control structures: Boolean expressions, selection control, iterative control; Lists: List structures, Lists, (sequences), iterating over lists. |
| **Module-3** | Functions: Program routines, calling value-returning functions, calling non value-returning functions, parameter passing, variable scope. |
| **Module-4** | Dictionaries and Sets; Recursion; Text Files: Using text files, string passing, exception handling. |

BOOKS AND REFERENCES

1. Michael Urban and Joel Murach, Python Programming, Shroff/Murach, 2016

2. Mark Lutz, Programming Python, O`Reilly, 4th Edition, 2010

# Semester - II

# Semester-II

## Core-3

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Microcontrollers and Programmable Digital Signal Processors.** | **MVE-201C** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Identify the features of ARM Cortex-M3 processor and LPC 17xx microcontroller. |
| **CO-2** | Design of ARM Cortex-M3 processor and LPC 17xx microcontroller applications with interrupts. |
| **CO-3** | Identify and characterize architecture of Programmable DSP Processors. |
| **CO-4** | Develop small applications by utilizing the ARM processor core & DSP processor based platform. |
| **CO-5** | Develop applications using Code Composer Studio. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces<br>LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT. |
| **MODULE-2** | Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency. |
| **MODULE-3** | Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC Module, Barrel shifters, Introduction to TI DSP processor family. |
| **MODULE-4** | VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking. |

**References:**


- Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
- Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH , 2nd Edition
- Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
- Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
- Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
- Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments.


## Core-4

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **VLSI Design Verification and Testing** | **MVE-202C** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Understand the Front end design and verification techniques and create reusable test environments. |
| **CO-2** | Identify Data types, arrays, linked list and procedural statements, tasks, functions and void functions, routine arguments. |
| **CO-3** | Understand the basics of VLSI Design Verification and Testing using OOP in system verilog. |
| **CO-4** | Demonstrate randomization of functions in system verilog |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance. |
| **MODULE-2** | Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width. Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the test-bench and design: Separating the test-bench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions. |
| **MODULE-3** | SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a test-bench. |
| **MODULE-4** | Randomization: Introduction, What to randomize, Randomization in System Verilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions. Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration. |

**References:**


- Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
- M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and• Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
- IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware Design,Specification, and Verification Language).
- System Verilog website – www.systemverilog.org http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
- General reuse information and resources www.design-reuse.com
- OVM, UVM(on top of SV) www.verificationacademy.com
- Verification IP resources http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
- http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx.


## Professional Elective-3

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Memory Technologies** | **MVE-201E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Understand and design random access memory and subsystems. |

| | |
|---|---|
| **CO-2** | Identify read only memory, fault models, modes and mechanisms in semiconductor memories and their testing procedures. |
| **CO-3** | Demonstrate the state-of-the-art memory chip design. |
| **CO-4** | Understanding of memory hybrids. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs. DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers. |
| **MODULE-2** | Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate, EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories. Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure, Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing. |
| **MODULE-3** | Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory devices. |
| **MODULE-4** | Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging. |

**References:**


- Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience.
- Kiyoo Itoh, "VLSI memory chip design", Springer International Edition
- Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability , PHI.


## Professional Elective-3

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **SoC Design** | **MVE-202E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Identify and formulate a given problem in the framework of SoC based design approaches. |
| **CO-2** | Design and verify Application Specific Instruction set Processors (ASIP). |
| **CO-3** | Design low power SOC systems. |
| **CO-4** | Understand the role and concept of graph theory and its relevance to synthesizable constructs. |
| **CO-5** | Evaluate real time cellular phone network design. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | ASIC- Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts. |
| **MODULE-2** | NISC- NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation – A formal language for specification, compilation and synthesis of embedded processors. |
| **MODULE-3** | Simulation- Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues. Low power SoC design / Digital system, - Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static |

| | |
|---|---|
| | voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification. |
| **MODULE-4** | Synthesis – Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs. Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization. |

**References:**


- Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
- B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
- RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
- P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
- Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011.


## Professional Elective-3

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Low Power VLSI Design** | **MVE-203E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability. |
| **CO-2** | Characterize and model power consumption & understand the basic analysis methods. |
| **CO-3** | Demonstrate leakage sources and reduction techniques. |
| **CO-4** | Illustrate the clock distribution issues in VLSI crcuits. |
| **CO-5** | Understand Low Power Memory and Microprocessor Design System. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations. |
| **MODULE-2** | Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches. |
| **MODULE-3** | Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network. Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers. |
| **MODULE-4** | Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits. Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance. |

**References:**


- P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
- Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.
- J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.

- A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
- Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

**Professional Elective-4**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Communication Busses and Interfaces** | **MVE-204E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Identify serial bus suitable for a particular application based on their feature. |
| **CO-2** | Develop applications using RS232, RS485, I2C, SPI. |
| **CO-3** | Demonstrate CAN architecture, PCIe Configuration and Hardware protocols. |
| **CO-4** | Understand USB – data transfer types and device driver fundamentals. |
| **CO-4** | Identify the use of Data Streaming Serial Communication Protocol using fiber optic and copper cable. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Serial Busses - Physical interface, Data and Control signals, features, |
| **MODULE-2** | Limitations and applications of RS232, RS485, I2C, SPI. |
| **MODULE-3** | CAN - Architecture, Data transmission, Layers, Frame formats, applications. PCIe - Revisions, Configuration space, Hardware protocols, applications. |
| **MODULE-4** | USB - Transfer types, enumeration, Descriptor types and contents, Device driver. Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable. |

**References:**


- Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ", Lakeview Research, 2nd Edition
- Jan Axelson, "USB Complete", Penram Publications
- Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
- Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
- Serial Front Panel Draft Standard VITA 17.1 – 200x
- Technical references on www.can-cia.org, www.pcisig.com, www.usb.org


**Professional Elective-4**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Network Security and Cryptography** | **MVE-205E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Identify and utilize different forms of cryptography techniques. |
| **CO-2** | Compare number theory algorithms. |
| **CO-3** | Distinguish between private and public key cryptography. |
| **CO-4** | Demonstrate Authentication- IP and Web Security Encapsulating Security Payload. |
| **CO-5** | Understand System Security- Intruders Firewalls, Firewall Design Principles, Trusted Systems. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Security- Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques. |
| **MODULE-2** | Number Theory- Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic. |
| **MODULE-3** | Private-Key (Symmetric) Cryptography- Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.<br>Public-Key (Asymmetric) Cryptography - RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC. |
| **MODULE-4** | Authentication- IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.<br>System Security- Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems. |

**References:**


- William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
- Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
- Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
- Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
- Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.


## Professional Elective-4

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Physical Design Automation** | **MVE-206E** | **4 hrs/week** | **4** | **40 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Demonstrate automation process for VLSI System design. |
| **CO-2** | Understand performance issues in VLSI circuit layout. |
| **CO-3** | Differentiate global placement, timing-driven placement and global routing. |
| **CO-4** | Understand in-chip routing terminologies. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Introduction to VLSI Physical Design Automation. |
| **MODULE-2** | Standard cell, Performance issues in circuit layout, delay models Layout styles. |
| **MODULE-3** | Discrete methods in global placement. Timing-driven placement. Global Routing Via Minimization. |
| **MODULE-4** | Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing. Compaction, algorithms, Physical Design Automation of FPGAs. |

**References:**


1. VLSI Physical Design Automation: Theory and Practice by Habib Yosuf.
2. Physical Design Automation of VLSI Systems by Bryan Preas.
3. *VLSI Physical Design: From Graph Partitioning to Timing Closure*. Authors: Kahng, A.B., Lienig, J., Markov, I.L., Hu, J.
4. *VLSI physical design Automation(Theory and Practice) by Sadiq m Sait and Habib Youssef*.
5. Practical problems in VLSI physical design Automation by Sung Kyu Lim, Springer Publications.

**Sessional-1**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Term Paper Leading to Thesis** | **MVE-201S** | **4 hrs/week** | **2** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Identify the project of their expertise domain and interest. |
| CO-2 | Explain the recent trend of research and its recent developments through literature survey |
| CO3 | Make an in-depth study of a specific topic within suitable engineering design and specifications. |

**Syllabus Contents:**

The project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The course should have the following-

1) Identification of domain for research.
2) Literature review.
3) In-depth study for suitable engineering design and specifications.

**Sessional-2**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Design Project** | **MVE-202S** | **4 hrs/week** | **2** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Outline the points to formulate problem corresponding to the project topic |
| CO-3 | Develop know how to organize, scope, plan, do and act within a project thesis. |
| CO-4 | Define problem specific tools (i.e. hardware equipment and software) and its functionality. |

**Syllabus Contents:**

The project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The course should have the following-

1) Problem formulation.
2) Knowledge of how to organize, scope, plan, do and act within a project thesis.
3) Familiarity with specific tools (i.e. hardware equipment and software) relevant to the project selected.

# Semester - III

# Semester-III

## Sessional-3

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Thesis Report Interim** | **MVE-301S** | **8 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Understand that how to write thesis with good readability |
| CO-2 | Learn to write section wise. |
| CO-3 | Understand the skills needed while writing a thesis |
| CO-4 | Ensure the quality of thesis report |

| | |
|---|---|
| **Module-1** | Planning and Preparation, Clarifying contributions of other authors, summarizing your findings, paraphrasing and plagiarism, sections of your thesis. |
| **Module-2** | Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check. key skills are needed when writing a thesis, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a review of the literature. |
| **Module-3** | Skills are needed when writing about the methods and results, skills are needed when writing the discussion, skills are needed when writing the conclusions. |
| **Module-4** | Useful phrases, how to ensure thesis is as good as it could possibly be the first-time thesis writing. |

## Sessional-4

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Thesis Seminar Interim (Presentation and Viva Voce)** | **MVE-302S** | **8 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem. |
| **CO-2** | Identify from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design. |
| **CO-3** | Demonstrate the findings of their technical solution in a written report. |
| **CO-4** | Present the work in International/ National conference or reputed journals. |

**Syllabus Contents:**

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study.

**A. The dissertation should have the following-**

i) Relevance to social needs of society
ii) Relevance to value addition to existing facilities in the institute
iii) Relevance to industry need
iv) Problems of national importance
v) Research and development in various domain

**B. The student should complete the following:**

i) Literature survey Problem Definition
ii) Motivation for study and Objectives
iii) Preliminary design / feasibility / modular approaches
iv) Implementation and Verification
v) Report and presentation

**Sessional-5**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Technical Communication** | **MVE-303S** | **4 hrs/week** | **2** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Understand that how to improve your writing skills and level of readability |
| CO-2 | Learn about what to write in each section |
| CO-3 | Understand the skills needed when writing a Title |
| CO-4 | Ensure the good quality of paper at very first-time submission |

| | |
|---|---|
| **Module-1** | Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.<br><br>Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction |
| **Module-2** | Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check. key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature. |
| **Module-3** | Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions |
| **Module-4** | Useful phrases, how to ensure paper is as good as it could possibly be the first-time submission |

BOOKS AND REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)

2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press

3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook.

4. Adrian Wall work, English for Writing Research Papers, Springer New York DordrechtHeidelberg London, 2011

**Sessional-6**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Workshop and Seminars - I** | **MVE-304S** | **2 hrs/week** | **0** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Follow discussions, oral arguments, and presentations, noting main points or evidence and tracking threads through different comments |
| CO-2 | Prepare appropriately to participate effectively and offer substantive replies to others' arguments, comments, and questions, while remaining sensitive to the original speaker and the classroom audience |
| CO-3 | Speak and debate with an appreciation for complex social and technical sensibilities |
| CO-4 | Offer compelling, articulate oral arguments, showing an understanding of the unique demands of oral presentation as opposed to writing |

**Syllabus Contents:**

1. Participate effectively in discussion of workshops and seminars [at least 02(two)].
2. Follow discussions, oral arguments, and presentations, noting main points or evidence and tracking threads through different comments and submit a comprehensive report to the department.
3. Demonstration of the ability to speak and defend (to be presented in the presentation seminar organized by the department).
4. Understanding of the unique demands of oral presentation as opposed to writing.( presentation skills will be evaluated)
5. Those who are unable to attend seminar / conferences/ workshops within the semester period needs to pass at least 01(one) NPTEL / MOOCs course of at least 04(four) weeks duration which should be relevant to project and thesis topic. Grade/ percentage of marks obtained in the NPTEL / MOOCs course examination will be proportionately taken into account for final evaluation of sessional -6.

**Professional Elective-5**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Internet of Things** | **MVE-301E** | **4 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Identify the IoT networking components with respect to OSI layer. |
| **CO-2** | Design and develop IoT based sensor systems. |
| **CO-3** | Select IoT protocols and software. |
| **CO-4** | Evaluate the wireless technologies for IoT. |
| **CO-5** | Identify essential requirements of IoT security |

| | |
|---|---|
| **MODULE-1** | **Evolution of IOT:** Review of computer communication concepts (OSI layers, components, packet communication, Networks, TCP-IP, subnetting,IPV4 addressing and challenges). IPV6 addressing. IoT architecture reference layer |
| **MODULE-2** | **Introduction to IoT components:** Characteristics IoT sensor nodes, Edge computer, cloud and peripheral cloud, single board computers, open source hardwares, Examples of IoT infrastructure. |
| **MODULE-3** | **IoT protocols and softwares:** MQTT, UDP, MQTT brokers, publish subscribe modes, HTTP, COAP,XMPP and gateway protocols.<br>**IoT point to point communication technologies:** IoT Communication Pattern, IoT protocol Architecture, Selection of Wireless technologies (6LoWPAN, Zigbee, WIFI, BT, BLE,SIG,NFC, LORA, Lifi, Widi) |
| **MODULE-4** | **IoT security:** Need for encryption, standard encryption protocol, light weight cryptography, Quadruple Trust Model for IoT-A – Threat Analysis and model for IoT-A, Cloud security<br>**IoT application and its Variants:** Case studies: IoT for smart cities, health care, agriculture, smart meters.M2M, Web of things, Cellular IoT, Industrial IoT, Industry 4.0,IoT standards. |

**TEXT BOOKS:**

1. The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers

**REFERENCES:**

1. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann
2. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, Huansheng Ning
3. Internet of Things (A Hands-on-Approach) , Vijay Madisetti , Arshdeep Bahga
4. Designing the Internet of Things , Adrian McEwen (Author), Hakim Cassimally
5. Asoke K Talukder and Roopa R Yavagal, "Mobile Computing," Tata McGraw Hill, 2010.
6. Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4 th Edition
7. Data and Computer Communications; By: Stallings, William; Pearson Education Pte. Ltd., Delhi, 6th Edition
8. F. Adelstein and S.K.S. Gupta, "Fundamentals of Mobile and Pervasive Computing," McGraw Hill, 2009.
9. Cloud Computing Bible, Barrie Sosinsky, Wiley-India, 2010
10. Cloud Security: A Comprehensive Guide to Secure Cloud Computing, Ronald L. Krutz, Russell Dean Vines, Wiley-India,

**Professional Elective-5**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Wireless Technologies** | **MVE-302E** | **4 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Demonstrate the fundament concepts of RF antenna design and spread spectrum |
| **CO-2** | Identify the different cellular technologies available today. |
| **CO-3** | Identify regulatory bodies and standards for WLAN Wi-Fi. |
| **CO-4** | Evaluate the Wi-Fi hardware and software. |
| **CO-5** | Elaborate Bluetooth technology aspects, interfacing problems with sensors and routing protocols. |

| | |
|---|---|
| **MODULE-1** | **Radio Frequency (RF) Fundamentals**: Spread Spectrum Concepts, RF Antenna concepts. **Cellular Standards**: Cellular carriers and Frequencies, Channel allocation, Cell coverage, Cell Splitting, Microcells, Picocells, Handoff 1st, 2nd, 3rd and 4th Generation Cellular Systems (GSM, CDMA,IS-95, GPRS, EDGE,UMTS, EVDO, CDMA2000), Mobile IP, WCDMA |
| **MODULE-2** | **WLAN Wi-Fi Organizations and Standards**: Regulatory Bodies, IEEE, Wi-Fi Alliance, WLAN Connectivity, WLAN QoS & Power-Save, IEEE 802.11 Standards,802.11-2007,802.11a/b/g, 802.11e/h/I,802.11n |
| **MODULE-3** | **Wi-Fi Hardware & Software:** Access Points, WLAN Routers, WLAN Bridges, WLAN Repeaters, WLAN Controllers/Switches, Direct-connect Aps, Distributed-connect Aps, PoE Infrastructure, Midspan, Endpoint, Client hardware and software, Antenna types and uses Wi-Fi Security concepts, Wi-Fi Applications. |
| **MODULE-4** | **WSN & WPN:** Wireless Personal Area Networks, Bluetooth, Bluetooth Standards, BlueTooth Protocol Architecture, UWB, IEEE 802.15 standards, ZigBee, Sub1GHz, Sensor Networks, Routing protocols in Wireless Sensor Networks. |

**TEXT BOOKS:**

1. Wireless Communications – Principles and Practice; by Theodore S Rappaport, Pearson Education Pte. Ltd., Delhi
2. Wireless Communications and Networking; By: Stallings, William; Pearson Education Pte. Ltd., Delhi

**REFERENCES:**

1. Bluetooth Revealed; By: Miller, Brent A, Bisdikian, Chatschik; Addison Wesley Longman Pte Ltd., Delhi
2. Wilson , "Sensor Technology hand book," Elsevier publications 2005.
3. Andrea Goldsmith, "Wireless Communications," Cambridge University Press, 2005
4. Mobile and Personal Communications Services and Systems; 1 st Edition; By: Raj Pandya; PHI, New Delhi
5. Fundamentals of Wireless Communication by Tse David and Viswanath Pramod, Cambridge University press, Cambridge
6. Mobile Communications; By: Schiller, Jochen H; Addison Wesley Longman Pte Ltd., Delhi
7. 3G Networks: Architecture, protocols and procedures based on 3GPP specifications for UMTS WCDMA networks, By Kasera, Sumit, Narang, and Nishit, TATA MGH, New Delhi
8. Wireless Sensor Networks: information processing by approach, ZHAO, FENG, GUIBAS and LEONIDAS J, ELSEVIER, New Delhi
9. Holger Karl and Andreas Wiilig, "Protocols and Architectures for Wireless Sensor Networks" John Wiley & Sons Limited 2008.

**Professional Elective-5**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Cloud Computing** | **MVE-303E** | **4 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Analyze the components of cloud computing and its business perspective. |
| **CO-2** | Evaluate the various cloud development tools. |
| **CO-3** | Collaborate with real time cloud services. |
| **CO-4** | Identify the need and process for virtualization of clouds |
| **CO-5** | Illustrate the measures required to make the cloud service secure. |

| | |
|---|---|
| **MODULE-1** | **CLOUD INTRODUCTION** Cloud Computing Fundamentals: Cloud Computing definition, Types of cloud, Cloud services: Benefits and challenges of cloud computing, Evolution of Cloud Computing , usage scenarios and Applications , Business models around Cloud – Major Players in Cloud Computing - Issues in Cloud - Eucalyptus - Nimbus - Open Nebula, CloudSim. |
| **MODULE-2** | **CLOUD SERVICES AND FILE SYSTEM** Types of Cloud services: Software as a Service - Platform as a Service – Infrastructure as a Service - Database as a Service - Monitoring as a Service – Communication as services. Service providers- Google App Engine, Amazon EC2, Microsoft Azure, Sales force. Introduction to Map Reduce, GFS, HDFS, Hadoop Framework. |
| **MODULE-3** | **COLLABORATING WITH CLOUD** Collaborating on Calendars, Schedules and Task Management – Collaborating on Event Management, Contact Management, Project Management – Collaborating on Word Processing ,Databases – Storing and Sharing Files- Collaborating via Web-Based Communication Tools – Evaluating Web Mail Services – Collaborating via Social Networks – Collaborating via Blogs and Wikis. |
| **MODULE-4** | **VIRTUALIZATION FOR CLOUD** Need for Virtualization – Pros and cons of Virtualization – Types of Virtualization – System Vm, Process VM, Virtual Machine monitor – Virtual machine properties - Interpretation and binary translation, HLL VM - Hypervisors – Xen, KVM , VMWare, Virtual Box, Hyper-V.<br>**SECURITY, STANDARDS, AND APPLICATIONS** Security in Clouds: Cloud security challenges – Software as a Service Security, Common Standards: The Open Cloud Consortium – The Distributed management Task Force – Standards for application Developers – Standards for Messaging – Standards for Security, End user access to cloud computing, Mobile Internet devices and the cloud. |

TEXT BOOKS

1. Bloor R., Kanfman M., Halper F. Judith Hurwitz “Cloud Computing for Dummies” Wiley India Edition),2010.
2. John Ritting house & James Ransome, “Cloud Computing Implementation Management and Strategy”, CRC Press, 2010
3. Antohy T Velte ,Cloud Computing : “A Practical Approach”, McGraw Hill,2009.
4. Michael Miller, Cloud Computing: “Web-Based Applications That Change the Way You Work and Collaborate Online”, Que Publishing, August 2008.
5. James E Smith, Ravi Nair, “Virtual Machines”, Morgan Kaufmann Publishers, 2006

**Professional Elective-5**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Automotive Electronics** | **MVE-304E** | **4 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Understand the working of various subsystems of a modern automobile and compare various control strategies |
| **CO-2** | Demonstrate the interfacing requirements for various sensors and actuators; |
| **CO-3** | Illustrate the requirements of electronic and digital engine control systems; |
| **CO-4** | Design motion control and onboard and off board diagnostics system. |

| | |
|---|---|
| **MODULE-1** | Automotive fundamentals: Automotive physical configuration, Engine, ignition system, drive train, suspension, brakes, steering system. Systems approach to control and instrumentation: Characteristics of digital electronic system, Instruments, Control system. |
| **MODULE-2** | Basics of Electronic Engine control: Motivation for electronic engine control, concept of an electronic engine control, definition of engine performance terms, Engine Mapping, control strategy, electronic fuel control system, electronic ignition. Sensors and actuators: Air flow rate sensor, engine crank shaft angular position sensor, throttles angle sensor, temperature sensor, oxygen sensor, knock sensor. Automotive engine control actuators. |
| **MODULE-3** | Digital Engine control system: Digital Engine control features, control modes for fuel control, EGR control, Electronic ignition control, integrated engine control system. |
| **MODULE-4** | Vehicle motion control: Cruise control system, Antilock braking system, Electronic suspension system, Electronic steering control, automotive instrumentation, on board and off – board diagnostics, occupant protection systems. |

TEXT BOOK 1. William B. Ribbens "Understanding Automotive Electronics" 6th Edition, Newnes
REFERENCE 1. Betchtold., "Understanding Automotive Electronics" SAE, 1998

**Audit Course (Interdisciplinary Mandatory)**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Research Methodology and IPR** | **MID-301A** | **2 hrs/week** | **0** | **28 hours** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Understand and formulate research problem. |
| **CO-2** | Inculcate research ethics |
| **CO-3** | Classify Intellectual Property Right (IPR). |
| **CO-4** | Comprehend about Intellectual Property Right utility in general and engineering in particular. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations |
| **MODULE-2** | Effective literature studies approaches, analysis Plagiarism, and Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee. |
| **MODULE-3** | Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT. |
| **MODULE-4** | Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs. |

**References:**


- Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
- Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
- Mayall , "Industrial Design", McGraw Hill, 1992.
- Niebel , "Product Design", McGraw Hill, 1974.
- Asimov , "Introduction to Design", Prentice Hall, 1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
- T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008.

# Semester – IV

# Semester-IV

**Sessional-7**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Thesis Report Final** | **MVE-401S** | **8 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Understand that how to write thesis with good readability |
| CO-2 | Learn to write section wise. |
| CO-3 | Understand the skills needed while writing a thesis |
| CO-4 | Ensure the quality of thesis report |

| | |
|---|---|
| **Module-1** | Planning and Preparation, Clarifying contributions of other authors, summarizing your findings, paraphrasing and plagiarism, sections of your thesis. |
| **Module-2** | Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check. key skills are needed when writing a thesis, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a review of the literature. |
| **Module-3** | Skills are needed when writing about the methods and results, skills are needed when writing the discussion, skills are needed when writing the conclusions. |
| **Module-4** | Useful phrases, how to ensure thesis is as good as it could possibly be the first-time thesis writing. |

**Sessional-8**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Thesis Seminar Final (Presentation and Viva Voce)** | **MVE-402S** | **8 hrs/week** | **4** |

**At the end of the course, students will demonstrate the ability to-**

| | Course Outcome |
|---|---|
| **CO-1** | Synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem. |
| **CO-2** | Identify from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design. |
| **CO-3** | Demonstrate the findings of their technical solution in a written report. |

| | |
|---|---|
| **CO-4** | Present the work in International/ National conference or reputed journals. |

**Syllabus Contents:**

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study.

**A. The dissertation should have the following-**

vi) Relevance to social needs of society
vii) Relevance to value addition to existing facilities in the institute
viii) Relevance to industry need
ix) Problems of national importance
x) Research and development in various domain

**B. The student should complete the following:**

vi) Literature survey Problem Definition
vii) Motivation for study and Objectives
viii) Preliminary design / feasibility / modular approaches
ix) Implementation and Verification
x) Report and presentation

**Sessional-9**

| Name of the course | Course Code | Time/ Duration | Credit |
|---|---|---|---|
| **Workshop and Seminars - II** | **MVE-403S** | **2 hrs/week** | **2** |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Follow discussions, oral arguments, and presentations, noting main points or evidence and tracking threads through different comments |
| CO-2 | Prepare appropriately to participate effectively and offer substantive replies to others' arguments, comments, and questions, while remaining sensitive to the original speaker and the classroom audience |
| CO-3 | Speak and debate with an appreciation for complex social and technical sensibilities |
| CO-4 | Offer compelling, articulate oral arguments, showing an understanding of the unique demands of oral presentation as opposed to writing |

**Syllabus Contents:**

1. Participate effectively in discussion of workshops and seminars [at least 02(two)].
2. Follow discussions, oral arguments, and presentations, noting main points or evidence and tracking threads through different comments and submit a comprehensive report to the department.
3. Demonstration of the ability to speak and defend (to be presented in the presentation seminar organized by the department).

4. Understanding of the unique demands of oral presentation as opposed to writing.( presentation skills will be evaluated)
5. Those who are unable to attend seminar / conferences/ workshops within the semester period needs to pass at least 01(one) NPTEL / MOOCs course of at least 04(four) weeks duration which should be relevant to project and thesis topic. Grade/ percentage of marks obtained in the NPTEL / MOOCs course examination will be proportionately taken into account for final evaluation of sessional -9.

**Open Elective**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| Medical Image Processing | MDS- 401O | 4 hrs/week | 4 | 40 hours |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Gain knowledge about basic medical imaging modalities (Understanding) |
| CO-2 | Able to evaluate and validate medical image data (Evaluation) |
| CO-3 | Learn to segment and classify various medical image data using various machine learning and deep learning techniques (Comprehension) |
| CO-4 | Acquaintances with some recent advances through Case studies (Evaluation) |

| | |
|---|---|
| **Module-1** | Introduction to medical imaging modalities and image analysis software, Introduction to Medical Image Analysis, X Ray and CT Imaging, Magnetic Resonance Imaging, Ultrasound Imaging, Optical Microscopy and Molecular Imaging |
| **Module-2** | Feature extraction, segmentation, systematic evaluation and validation on datasets, Texture in Medical Images, Region Growing and Clustering, Random Walks for Segmentation, Active Contours for Segmentation |
| **Module-3** | Machine learning based approaches for segmentation and classification, Systematic Evaluation and Validation, Decision Trees for Segmentation and Classification, Random Forests for Segmentation and Classification, Neural Networks for Segmentation and Classification, Deep Learning for Medical Image Analysis |
| **Module-4** | Case studies on some recent advances in analysis of retinal, CT, MRI, ultrasound and histology images, Retinal Vessel Segmentation, Vessel Segmentation in Computed Tomography Scan of Lungs, Tissue Characterization in Ultrasound |

BOOKS AND REFERENCES:


1. swayam.gov.in
2. Guide to Medical Image Analysis: Methods and Algorithms, Klaus D. Toennies, Print ISBN: 978-1-4471-2750-5
3. Advancement of Machine Intelligence in Interactive Medical Image Analysis, Om Prakash Verma, Sudipta Roy, Subhash Chandra Pandey, Mamta Mittal, Print ISBN: 978-981-15-1099-1

**Open Elective**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| Data Warehousing | MDS- 402O | 4 hrs/week | 4 | 40 hours |

**At the end of the course, students will demonstrate the ability to-**

| | COURSE OUTCOMES |
|---|---|
| CO-1 | Evaluate of different sequential pattern algorithms |
| CO-2 | Realize the technique to extract patterns from time series data and its application in real world. |
| CO-3 | Apply the Graph mining algorithms to Web mining |
| CO-4 | Identify the computing framework for Big Data |

| | |
|---|---|
| **Module-1** | Introduction to Data Warehousing; Data Mining: Mining frequent patterns, association and correlations; Sequential Pattern Mining concepts, primitives, scalable methods; Classification and prediction; Cluster Analysis – Types of Data in Cluster Analysis, Partitioning methods, Hierarchical Methods; Transactional Patterns and other temporal based frequent patterns. |
| **Module-2** | Mining Time series Data, Periodicity Analysis for time related sequence data, Trend analysis, Similarity search in Time-series analysis |
| **Module-3** | Mining Data Streams, Methodologies for stream data processing and stream data systems, Frequent pattern mining in stream data, Sequential Pattern Mining in Data Streams, Classification of dynamic data streams, Class Imbalance Problem; Graph Mining; Social Network Analysis |
| **Module-4** | Web Mining, Mining the web page layout structure, mining web link structure, mining multimedia data on the web, Automatic classification of web documents and web usage mining; Distributed Data Mining.<br><br>Recent trends in Distributed Warehousing and Data Mining, Class Imbalance Problem; Graph Mining; Social Network Analysis techniques. |

BOOKS AND REFERENCES:

1. Jiawei Han and M Kamber, Data Mining Concepts and Techniques, Second Edition, Elsevier Publication, 2011.

2. Vipin Kumar, Introduction to Data Mining - Pang-Ning Tan, Michael Steinbach, Addison Wesley, 2006. 3. G Dong and J Pei, Sequence Data Mining, Springer, 2007.

**Open Elective**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Principles of Refrigeration and Cryogenics** | **MTE-401O** | **4 hrs/week** | **4** | **40 hours** |

**Course Outcomes:**

| At the end of the course students will be able to- | |
|---|---|
| **CO-1** | Learn the basics of refrigeration cycle and systems with its application area. |
| **CO-2** | Design the refrigeration systems through proper selection of compressors, evaporators and condensers. |
| **CO-3** | Learn about refrigerants, ODP, GWP and related environment issues. |
| **CO-4** | Analyze vapour absorption refrigeration, gas liquefaction systems and related applications. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Vapour compression refrigeration, actual cycle, second law efficiency, multistage compression with inter-cooling, multi-evaporator systems, cascade systems. |
| **MODULE-2** | Performance characteristics and capacity control of reciprocating and centrifugal compressors, screw compressor and scroll compressor, design, selection of evaporators, condensers, control systems, motor selection. |
| **MODULE-3** | Refrigerants, alternative refrigerants, CFC/HCFC phase-out regulations, refrigeration applications, food preservation, transport. |
| **MODULE-4** | Introduction to vapour absorption refrigeration, single effect and double effect systems, gas liquefaction systems - Linde-Hampson, Linde dual pressure, Claude cycle. |

**Book and References:**


1. 1. R.J.Dossat, "Principles of Refrigeration", Pearson Education Asia, 2001.
2. C.P.Arora, "Refrigeration and Air-conditioning", Tata McGraw-Hill, 2000.
3. Stoecker & Jones, "Refrigeration and Air-conditioning", McGraw Hill Book Company, New York, 1982.
4. Jordan & Priester, "Refrigeration and Air-conditioning".
5. A.R.Trott, "Refrigeration and Air-conditioning", Butterworths, 2000.
6. J.L.Threlkeld, "Thermal Environmental Engineering", Prentice Hall, 1970.
7. R.Barron, "Cryogenic systems", McGraw–Hill Company, New Yourk, 1985.
8. G.G.Hasseldon. "Cryogenic Fundamentals", Academic Press.
9. Bailey, "Advanced Cryogenics", Plenum Press, London, 1971.


**Open Elective**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Design and Application of Solar Thermal Systems** | **MTE-402O** | **4 hrs/week** | **4** | **40 hours** |

**Course Outcomes:**

| At the end of the course students will be able to- | |
|---|---|
| **CO-1** | Acquire the knowledge of different aspects and parameters of solar energy systems. |

| | |
|---|---|
| **CO-2** | Analyze the performance of various solar thermal systems. |
| **CO-3** | Design, test, model, optimize and analyze different solar drying systems and associated impacts. |
| **CO-4** | Generate the scenarios of recent advances and applications of SAH integrated with SHS and LHS in solar dryers and predict the future trends. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | **10 hours**<br>**Basics of Solar Thermal Systems:** Introduction to Solar Air Heater (SAH)**,** Different components of SAH; Radiation transmission and absorption through glazing; Selective surfaces: Ideal coating characteristics, Anti reflection coating, application of SAH in solar drying systems and case studies. |
| **MODULE-2** | **12 hours**<br>**Solar Air Heater or Collector and Thermal Energy Storage:** Flat Plate Collector: Theory and basic design aspects; Thermal analysis and effective heat loss; Performance analysis methods; Concentrating Collector: Classification of concentrating collector; concentrating collector configurations; Thermal performance of concentrating collector; Optical and thermal performance of different concentrating collector designs; Solar thermal energy storage: LSH and SHS materials, Designing thermal storage systems, recent advances in solar air heater methods, technologies with applications and future trends. |
| **MODULE-3** | **08 hours**<br>**Solar Drying Systems:** Basic concepts and classifications of Solar Drying systems (SDS), design, testing and modelling of SDS, environomical impact of SDS, innovations in SDS, `4 E` analysis of SDS, heat and moisture transfer and optimization of SDS. |
| **MODULE-4** | **10 hours**<br>**Applications of Solar Thermal Systems:** Performance evaluation of Solar Dryer with SHS and SAH: design, fabrication and detailed instrumentation of solar dryer, Mathematical modelling of SAH, Performance of SAH and Solar Dryer, Environomical analysis and future trends. Performance analysis of Solar Dryer integrated with LHS and SAH: design, fabrication and detailed instrumentation, energy and exergy analysis, performance test of solar dryer, future trends. |

**Books and References:**


1. Duffie J. A. and Beckman W. A. (2013); *Solar Engineering of Thermal Processes*, John Wiley
2. Garg H. P. and Prakash S. (2000); *Solar Energy: Fundamental and Application*, Tata McGraw Hill
3. Nayak J. K. and Sukhatme S. P. (2006); Solar Energy: Principles of Thermal Collection and Storage, Tata McGraw Hill
4. Twidell J, Weir T (2015); *Renewable Energy Resources*, Routledge
5. Dincer I., and Rosen M. A. (2011); *Thermal Energy Storage: Systems and Applications*, Wiley
6. Dinçer, İ. and Zamfirescu, C., 2016. *Drying phenomena: theory and applications*. John Wiley & Sons.
7. Prakash, O. and Kumar, A. eds., 2017. *Solar drying technology: concept, design, testing, modeling, economics, and environment*. Springer.

8. Ataer, O.E., 2009. Storage of thermal energy. Energy storage systems, 1, p.97.

Tyagi, H., Chakraborty, P.R., Powar, S. and Agarwal, A.K. eds., 2019. *Solar*

**Foundation Course**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **English for research paper writing** | **MID-401F** | **2 hrs/week** | **0** | **20 hours** |

**Course Outcomes:**

| At the end of the course students will be able to- | |
|---|---|
| **CO-1** | Identify scope to improve writing skills and level of readability. |
| **CO-2** | Demonstrate technical paper writing skills. |
| **CO-3** | Develop the skills to write a good quality of paper. |
| **CO-4** | Present the Literature review, Methods, Results, Discussion, Conclusions and Final Check in result oriented manner. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness. |
| **MODULE-2** | Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction |
| **MODULE-3** | Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check. key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, |
| **MODULE-4** | Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the conclusions. Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission. |

**References:**


- Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books).
- Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press.
- Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook .
- Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.


**Foundation Course**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Disaster management** | **MID-402F** | **2 hrs/week** | **0** | **20 hours** |

**Course Outcomes:**

| At the end of the course students will be able to- | |
|---|---|
| **CO-1** | Demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response. |
| **CO-2** | Understand Repercussions Of Disasters And Hazards. |
| **CO-3** | Illustrate natural and manmade disasters. |
| **CO-4** | Classify disaster prone areas in India. |
| **CO-5** | Analysis of disaster risk assessment and reduction mechanisms. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude. |
| **MODULE-2** | Repercussions Of Disasters And Hazards: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts. |
| **MODULE-3** | Disaster Prone Areas In India Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics. Disaster Preparedness And Management Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And CommModuley Preparedness. |
| **MODULE-4** | Risk Assessment Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.Disaster Mitigation Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India. |

**References:**


- R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
- Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
- Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., New Delhi.


## Foundation Course

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Sanskrit for technical knowledge** | **MID-403F** | **2 hrs/week** | **0** | **20 hours** |

**Course Outcomes:**

| At the end of the course students will be able to- | |
|---|---|
| **CO-1** | Develop a working knowledge in illustrious Sanskrit, the scientific language in the world |
| **CO-2** | Learn Sanskrit to improve brain functioning |
| **CO-3** | Develop the logic in mathematics, science & other subjects enhancing the memory power |
| **CO-4** | Explore the technical knowledge from ancient literature. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences. |
| **MODULE-2** | Order, Introduction of roots. |
| **MODULE-3** | Technical information about Sanskrit Literature. |
| **MODULE-4** | Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics. |

**References:**


- "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
- "Teach Yourself Sanskrit" Prathama Deeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, NewDelhi Publication
- "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.


**Foundation Course**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Value Education** | **MID-404F** | **2 hrs/week** | **0** | **20 hours** |

**Course Outcomes:**

| **At the end of the course students will be able to-** | |
|---|---|
| **CO-1** | Understand value of education and self- development. |
| **CO-2** | Imbibe good values in students. |
| **CO-3** | Inculcate about the importance of character. |
| **CO-4** | Demonstrate mind training, Self-control, Honesty, Studying effectively. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Values and self-development –Social values and individual, attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements |
| **MODULE-2** | Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Moduley. Patriotism. Love for nature ,Discipline |
| **MODULE-3** | Personality and Behavior Development – Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature |
| **MODULE-4** | Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively. |

**References:**


- Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi


**Foundation Course**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Constitution of India** | **MID-405F** | **2 hrs/week** | **0** | **20 hours** |

**Course Outcomes:**

| At the end of the course, students will be able to- | |
|---|---|
| **CO-1** | Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective. |
| **CO-2** | Understand the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism. |
| **CO-3** | Understand the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution. |
| **CO-4** | Demonstratethe Role and Functioning ofElection Commission,. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | History of Making of the Indian Constitution: History Drafting Committee, ( Composition & Working) |
| **MODULE-2** | Philosophy of the Indian Constitution: Preamble, Salient Features. Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties. |
| **MODULE-3** | Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy. |
| **MODULE-4** | Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women. |

**References:**


- The Constitution of India, 1950 (Bare Act), Government Publication.
- Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
- M. P. Jain, Indian Constitution Law, 7thEdn., Lexis Nexis, 2014.
- D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.


**Foundation Course**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Pedagogy studies** | **MID-406F** | **2 hrs/week** | **0** | **20hours** |

**Course Outcomes:**

| At the end of the course students will be able to- | |
|---|---|
| **CO-1** | Understand parameters and terminology of pedagogy. |
| **CO-2** | Compare pedagogical practices in developing countries. |
| **CO-3** | Measure effectiveness of pedagogical practices. |
| **CO-4** | Assess Professional development by alignment with classroom practices and follow-up support and Peer support. |
| **CO-5** | Identify Research gaps and future directions, Research design, Contexts, Pedagogy,etc. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology. Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching. |
| **MODULE-2** | Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education. |
| **MODULE-3** | Evidence on the effectiveness of pedagogical practices. Methodology for the in depth stage: quality assessment of included, studies. How can teacher education (curriculum and practicum) and the school, curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical.practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies. |
| **MODULE-4** | Professional development: alignment with classroom practices and follow-up support Peer support. Support from the head teacher and the commModuley. Curriculum and assessment. Barriers to learning: limited resources and large class sizes.Research gaps and future directions, Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact. |

**References:**


- Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
- Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
- Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
- Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
- Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
- Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
- www.pratham.org/images/resource%20working%20paper%202.pdf.


**Foundation Course**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Stress Management by Yoga** | **MID-407F** | **2 hrs/week** | **0** | **20 hours** |

**Course Outcomes:**

| At the end of the course students will be able to- |
|---|

| | |
|---|---|
| **CO-1** | Understand the role of yoga in developing overall health of body and mind. |
| **CO-2** | Understand the importance of Yoga in Overcoming stress. |
| **CO-3** | Experiment with various asanas and Pranayams. |
| **CO-4** | Implement breathing techniques. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Definitions of Eight parts of yog. ( Ashtanga ) |
| **MODULE-2** | Yam and Niyam. Do`s and Don't's in life. I) Ahinsa, satya, astheya, bramhacharya and aparigraha ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan. |
| **MODULE-3** | Asan and Pranayam- Various yog poses and their benefits for mind & body. |
| **MODULE-4** | Regularization of breathing techniques and its effects-Types of pranayam |

**References:**


- 'Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal, Nagpur
- "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata


**Foundation Course**

| Name of the course | Course Code | Time/ Duration | Credit | Total Classes |
|---|---|---|---|---|
| **Personality Development Through Life Enlightenment Skills** | **MID-408F** | **2 hrs/week** | **0** | **20 hours** |

**Course Outcomes:**

| **At the end of the course students will be able to-** | |
|---|---|
| **CO-1** | Understand the skill to achieve the highest goal happily. |
| **CO-2** | Develop the skills of a person with stable mind, pleasing personality and determination. |
| **CO-3** | Inculcate wisdom in them. |
| **CO-4** | Understand basic knowledge of Shrimad BhagwadGeeta. |

**Syllabus Contents:**

| | |
|---|---|
| **MODULE-1** | Neetisatakam-Holistic development of personality Verses- 19,20,21,22 (wisdom), Verses-29,31,32 (pride & heroism) Verses- 26,28,63,65 (virtue), Verses- 52,53,59 (dont's), Verses-71,73,75,78 (do's). |
| **MODULE-2** | Approach to day to day work and duties. Shrimad BhagwadGeeta : Chapter 2-Verses 41, 47,48, Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, Chapter 18-Verses 45, 46, 48. |
| **MODULE-3** | Statements of basic knowledge. Shrimad BhagwadGeeta: Chapter2-Verses 56, 62, 68, Chapter 12 -Verses 13, 14, 15, 16,17, 18. |
| **MODULE-4** | Personality of Role model. Shrimad BhagwadGeeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, Chapter 4-Verses 18, 38,39, Chapter18 – Verses 37,38,63. |

**References:**


- "Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication Department), Kolkata

- Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.